

CLAIMS

What is claimed is:

1 1. A scalable digital loop carrier system
2 capable of providing voice, video and data
3 communications, the system comprising:

4
5 (a) a primary channel bank;

6
7 (b) an asynchronous transfer mode (ATM)
8 interface connected to the primary channel bank;

9
10 (c) a time division multiplex (TDM)
11 interface connected to the primary channel bank; and

12
13 (d) at least a first secondary channel bank
14 connected to the primary channel bank through the ATM
15 and TDM interfaces, the primary channel bank capable of
16 providing clock synchronization to the secondary
17 channel bank, wherein the primary channel bank and the
18 secondary channel bank each comprise:

19
20 (i) a time slot cross-connect
21 interchanger (TSI) having a plurality of subscriber bus
22 interfaces; and

23

25

24 (ii) an ATM access controller
25 connected to the TSI, the ATM access controller having
26 a plurality of ATM cell bus interfaces.

1 2. The system of claim 1, wherein the primary
2 channel bank further comprises a synchronous transport
3 signal (STS)⁹⁶ cross-connect controller connected to the
4 TSI in the primary channel bank.

1 3. The system of claim 2, wherein the primary
2 channel bank further comprises a synchronous optical
3 network (SONET) framer connected to the STS cross-
4 connect controller in the primary channel bank.

1 4. The system of claim 2, further comprising a
2 plurality of STS transport cards connected to the STS
3 cross-connect controller in the primary channel bank.

1 5. The system of claim 1, wherein the secondary
2 channel bank further comprises a synchronous transport
3 signal (STS) cross-connect controller connected to the
4 TSI in the secondary channel bank.

1 6. The system of claim 5, wherein the secondary
2 channel bank further comprises a synchronous optical

3 network (SONET) framer connected to the STS cross-
4 connect controller in the secondary channel bank.

1 7. The system of claim 5, further comprising a
2 plurality of STS transport cards connected to the STS
3 cross-connect controller in the secondary channel bank.

1 8. The system of claim 1, wherein the TDM
2 interface is capable of supporting 16 time division
3 multiplexed channels.

1 9. The system of claim 1, wherein the ATM
2 interface is capable of transporting 216 ATM cells per
3 125 μ s frame.

1 10. The system of claim 1, wherein the TDM
2 interface is capable of providing a plurality of
3 synchronous transport signal-one (STS-1) channels in a
4 synchronous optical network (SONET) frame.

1 11. The system of claim 1, wherein the primary
2 channel bank further comprises a timing generator to
3 provide timing reference to the TSI and ATM access
4 controllers in the primary channel bank, the timing
5 generator having a timing reference input and a clock

6 synchronization output connected to the secondary
7 channel bank.

1 12. The system of claim 11, wherein the timing
2 reference input comprises a synchronous optical network
3 (SONET) timing reference input.

1 13. The system of claim 11, wherein the timing
2 reference input comprises a T1 timing reference input.

1 14. The system of claim 11, wherein the timing
2 reference input comprises a building integrated timing
3 supply (BITS) input.

1 15. The system of claim 11, wherein the secondary
2 channel bank further comprises a timing generator to
3 provide timing reference to the TSI and the ATM access
4 controller in the secondary channel bank, the timing
5 generator in the secondary channel bank synchronized by
6 a clock synchronization signal received from the clock
7 synchronization output of the primary channel bank.

1 16. The system of claim 1, further comprising a
2 second secondary channel bank connected to the primary
3 channel bank through the TDM and ATM interfaces.

1 17. The system of claim 16, wherein the second
2 secondary channel bank is connected to the first
3 secondary channel bank through the TDM and ATM
4 interfaces.

1 ~~18~~. A scalable digital loop carrier system
2 capable of providing voice, video and data
3 communications, the system comprising:
4

5 (a) a primary channel bank;
6

7 (b) an asynchronous transfer mode (ATM)
8 interface connected to the primary channel bank;
9

10 (c) a time division multiplex (TDM)
11 interface connected to the primary channel bank; and
12

13 (d) at least a first secondary channel bank
14 connected to the primary channel bank through the ATM
15 and TDM interfaces, the primary channel bank capable of
16 providing clock synchronization to the secondary
17 channel bank, wherein the primary channel bank and the
18 secondary channel bank comprise respective node control
19 processors capable of communicating to each other, each
20 of the node control processors comprising:
21

22 (i) a time slot cross-connect
23 interchanger (TSI) having a plurality of subscriber bus
24 interfaces;

25

26 (ii) an ATM access controller
27 connected to the TSI, the ATM access controller having
28 a plurality of ATM cell bus interfaces;

29

30 (iii) a synchronous transport signal
31 (STS) cross-connect controller connected to the TSI;
32 and

33

34 (iv) a synchronous optical network
35 (SONET) framer connected to the STS cross-connect
36 controller.

1 19. The system of claim 18, further comprising a
2 plurality of STS transport cards connected to the STS
3 cross-connect controller in the primary channel bank.

1 20. The system of claim 18, further comprising a
2 plurality of STS transport cards connected to the STS
3 cross-connect controller in the secondary channel bank.

1 21. The system of claim 18, wherein the STS
2 cross-connect controller is capable of supporting at
3 least 12 STS-1 channels.

1 22. The system of claim 18, wherein the TDM
2 interface is capable of providing a plurality of
3 synchronous transport signal-one (STS-1) channels in a
4 synchronous optical network (SONET) frame.

1 23. The system of claim 18, wherein the primary
2 channel bank further comprises a timing generator to
3 provide timing reference to the TSI and the ATM access
4 controller in the primary channel bank, the timing
5 generator having a timing reference input and a clock
6 synchronization output connected to the secondary
7 channel bank.

1 24. The system of claim 23, wherein the timing
2 reference input comprises a synchronous optical network
3 (SONET) timing reference input.

1 25. The system of claim 23, wherein the timing
2 reference input comprises a T1 timing reference input.

1 26. The system of claim 23, wherein the timing
2 reference input comprises a building integrated timing
3 supply (BITS) input.

1 27. The system of claim 23, wherein the secondary
2 channel bank further comprises a timing generator to
3 provide timing reference to the TSI, the STS cross-
4 connect controller and the ATM access controller in the
5 secondary channel bank, the timing generator in the
6 secondary channel bank synchronized by a clock
7 synchronization signal received from the clock
8 synchronization output of the primary channel bank.

9
10 28. The system of claim 18, further comprising a
11 second secondary channel bank connected to the primary
12 channel bank through the TDM and ATM interfaces.

1 29. The system of claim 28, wherein the second
2 secondary channel bank is connected to the first
3 secondary channel bank through the TDM and ATM
4 interfaces.

1 30. The system of claim 18, wherein each of the
2 node control processors further comprises a
3 microprocessor connected to the TSI and the ATM access
4 controller.

1 31. The system of claim 30, wherein each of the
2 node control processors further comprises a data link
3 and control tone card (DCT) connected to the
4 microprocessor.

1 32. A scalable digital loop carrier system
2 capable of providing voice, video and data
3 communications, the system comprising:
4

5 (a) a primary channel bank;
6

7 (b) an asynchronous transfer mode (ATM)
8 interface connected to the primary channel bank;
9

10 (c) a time division multiplex (TDM)
11 interface connected to the primary channel bank; and
12

13 (d) at least a first secondary channel bank
14 connected to the primary channel bank through the ATM
15 and TDM interfaces, wherein the primary channel bank
16 and the secondary channel bank each comprise:
17

18 (i) a time slot cross-connect
19 interchanger (TSI) having a plurality of subscriber bus
20 interfaces;

21 (ii) an ATM access controller
22 connected to the TSI, the ATM access controller having
23 a plurality of ATM cell bus interfaces; and
24

25 (iii) a timing generator to provide
26 timing reference to the TSI and the ATM access
27 controller, the timing generator in the primary channel
28 bank having a timing reference input and a clock
29 synchronization output connected to provide clock
30 synchronization to the timing generator in the
31 secondary channel bank.
32

33 33. The system of claim 32, wherein the primary
34 channel bank further comprises a synchronous transport
35 signal (STS) cross-connect controller connected to the
36 TSI in the primary channel bank.

1 34. The system of claim 33, wherein the primary
2 channel bank further comprises a synchronous optical
3 network (SONET) framer connected to the STS cross-
4 connect controller in the primary channel bank.

1 35. The system of claim 33, further comprising a
2 plurality of STS transport cards connected to the STS
3 cross-connect controller in the primary channel bank.

1 36. The system of claim 32, wherein the secondary
2 channel bank further comprises a synchronous transport
3 signal (STS) cross-connect controller connected to the
4 TSI in the secondary channel bank.

1 37. The system of claim 36, wherein the secondary
2 channel bank further comprises a synchronous optical
3 network (SONET) framer connected to the STS cross-
4 connect controller in the secondary channel bank.

1 38. The system of claim 36, further comprising a
2 plurality of STS transport cards connected to the STS
3 cross-connect controller in the secondary channel bank.

1 39. The system of claim 32, wherein the TDM
2 interface is capable of supporting 16 time division
3 multiplexed channels.

1 40. The system of claim 32, wherein the ATM
2 interface is capable of transporting 216 ATM cells per
3 125 μ s frame.

1 41. The system of claim 32, wherein the TDM
2 interface is capable of providing a plurality of
3 synchronous transport signal-one (STS-1) channels in a
4 synchronous optical network (SONET) frame.

1 42. The system of claim 32, wherein the timing
2 reference input of the timing generator in the primary
3 channel bank comprises a synchronous optical network
4 (SONET) timing reference input.

1 43. The system of claim 32, wherein the timing
2 reference input of the timing generator in the primary
3 channel bank comprises a T1 timing reference input.

1 44. The system of claim 32, wherein the timing
2 reference input of the timing generator in the primary
3 channel bank comprises a building integrated timing
4 supply (BITS) input.

1 45. The system of claim 32, further comprising a
2 second secondary channel bank connected to the primary
3 channel bank through the TDM and ATM interfaces.

1 46. The system of claim 45, wherein the second
2 secondary channel bank is connected to the first
3 secondary channel bank through the TDM and ATM
4 interfaces.

1 47. A scalable digital loop carrier system
2 capable of providing voice, video and data
3 communications, the system comprising:

4
5 (a) a primary channel bank;

6
7 (b) an asynchronous transfer mode (ATM)
8 interface connected to the primary channel bank;

9
10 (c) a time division multiplex (TDM)
11 interface connected to the primary channel bank; and

12
13 (d) a plurality of secondary channel banks
14 connected to the primary channel bank through the ATM
15 and TDM interfaces, wherein the primary channel bank
16 and the secondary channel banks comprise respective
17 timing generators and respective node control
18 processors,

19
20 wherein the timing generators are
21 capable of providing clock signals for the respective
22 channel banks, the timing generator in the primary
23 channel bank having a timing reference input and a
24 clock synchronization output connected to provide clock
25 synchronization to the timing generators in the
26 secondary channel banks, and

27 wherein the node control processors each
28 comprise:

29
30 (i) a time slot cross-connect
31 interchanger (TSI) having a plurality of subscriber bus
32 interfaces;

33
34 (ii) an ATM access controller
35 connected to the TSI, the ATM access controller having
36 a plurality of ATM cell bus interfaces;

37
38 (iii) a synchronous transport signal
39 (STS) cross-connect controller connected to the TSI;
40 and

41
42 (iv) a synchronous optical network
43 (SONET) framer connected to the STS cross-connect
44 controller.

1 48. The system of claim 47, further comprising a
2 plurality of STS transport cards connected to the STS
3 cross-connect controller in the primary channel bank.

1 49. The system of claim 47, further comprising a
2 plurality of STS transport cards connected to the STS

3 cross-connect controller in the secondary channel
4 banks.

1 50. The system of claim 47, wherein the STS
2 cross-connect controller is capable of supporting at
3 least 12 STS-1 channels.

1 51. The system of claim 47, wherein the TDM
2 interface is capable of providing a plurality of
3 synchronous transport signal-one (STS-1) channels in a
4 synchronous optical network (SONET) frame.

1 52. The system of claim 47, wherein the timing
2 reference input of the timing generator in the primary
3 channel bank comprises a synchronous optical network
4 (SONET) timing reference input.

1 53. The system of claim 47, wherein the timing
2 reference input of the timing generator in the primary
3 channel bank comprises a T1 timing reference input.

1 54. The system of claim 47, wherein the timing
2 reference input of the timing generator in the primary
3 channel bank comprises a building integrated timing
4 supply (BITS) input.

1 55. The system of claim 47, wherein each of the
2 node control processors further comprises a
3 microprocessor connected to the TSI and the ATM access
4 controller.

1 56. The system of claim 55, wherein each of the
2 node control processors further comprises a data link
3 and control tone card (DCT) connected to the
4 microprocessor.